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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,886	SAHA, BRATIN	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *March 9th, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-34 have been examined.

Acknowledgment of papers filed: oath, specification, drawings, and IDS, on March 9th, 2004. The papers filed have been placed on record.

Specification

2. The title is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 16-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 16-20 disclose an "article comprising a machine-readable medium". This language potentially includes non-tangible and, therefore, non-statutory subject matter. Examiner suggests rephrasing the language to disclose "an article comprising a machine-readable storage medium".

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 11, 12, 15, 16, 17, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Rajwar (Speculative Lock Elision).

6. Regarding claim 11, Rajwar discloses a machine-implemented method comprising: generating parallel processes in a data processing machine (Rajwar page 294 col 1 section 1); effecting synchronization between the parallel processes using processor speculation in the data processing machine (Rajwar page 295 col 1); and providing output resulting from the synchronized parallel processes (Rajwar page 294 col 2 second paragraph).

Note the use of a store instruction. This is considered to be a readable output.

7. Regarding claim 12, Rajwar discloses the method of claim 11, wherein said generating parallel processes comprises running a software program (Rajwar page 294 figure 1) that spawns multiple threads in the data processing machine (Rajwar page 294 section 1 col 1).

8. Regarding claim 15, Rajwar discloses the method of claim 11, wherein said providing output comprises sending the output to another data processing machine (Rajwar page 294 section 1 col 1).

Note that the store instructions within a processor stores data to memory. This output is then picked up by another processor in the "shared memory multiprocessors" disclosed in Rajwar.

9. Regarding claim 16, Rajwar discloses an article comprising a machine-readable medium embodying information indicative of instructions that when performed by one or more machines result in operations (Rajwar page 294 col 2 fig 1)

Note that clearly, the instructions disclosed in figure 1 must be contained on a computer readable medium for the processing system to execute the instructions.

Comprising: generating parallel processes in a data processing machine (Rajwar page 294 col 1 section 1); effecting synchronization between the parallel processes using processor speculation in the data processing machine (Rajwar page 295 col 1); and providing output resulting from the synchronized parallel processes (Rajwar page 294 col 2 "store instruction").

10. Regarding claim 17, Rajwar discloses the article of claim 16, wherein said generating parallel processes comprises running a software program that spawns multiple threads in the data processing machine (Rajwar page 294 section 1 col 1).

11. Regarding claim 20, Rajwar discloses the article of claim 16, wherein said providing output comprises sending the output to another data processing machine (Rajwar page 294 section 1 col 1).

Note: see claim 15

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1, 6, 7, 14, 19, 21-27, and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajwar in view of Lam (Enhancing Software Reliability with Speculative Threads).

14. Regarding claim 1, Rajwar discloses a processor (Rajwar page 294 Section 1 first 4 lines) comprising: a front end that obtains instructions (see below);

Note that the terms, "front end" and "back end", as vaguely defined are limited only by how the reference is defined. Any portion of the processor can be considered a "front end" or "back end".

And a back end that provides speculative execution of the instructions (Rajwar page 295 third paragraph);

Rajwar fails to disclose an instruction that follows all claimed limitations.

Lam discloses an instruction set architecture including speculative execution control circuitry that handles at least one machine instruction that facilitates

synchronization between parallel processes by exposing the processor speculation to program control (Lam page 187 TRY instruction).

Although it is clear from Rajwar that synchronization is maintained, it does not describe a particular instruction for doing so. Lam, however, uses this TRY instruction which "allows the program to recover from attacks that overwrite data structures beyond those expected". Rajwar would be motivated to use this technique because it gives a large amount of control to the programmer, who can remove unnecessary processor commands (which happened to be the general motivation behind the Rajwar invention initially). Additionally, for the same motivation, Rajwar would be motivated to include other elements of lock speculation in an explicit instruction.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the processing system of Rajwar maintain synchronization through explicit instructions such as TRY, COMMIT, and ABORT, as in Lam.

15. Regarding claim 6, Rajwar/Lam discloses the processor of claim 1, wherein the at least one machine instruction comprises: a speculative execution instruction that takes first and second operands,

Note that the term "operands" most commonly refers to inputs of an arithmetic operation. Applicant's invention does not use the claimed operands for that purpose. Consequently, Examiner believes it is reasonable to consider the claimed operands to be any register associated to the instruction.

Behaves as a no-op if a memory location indicated by the first operand contains a first value (Lam page 187 section 3.2),

Note that the TRY instruction serves no purpose if there is no error.

Causes the processor to speculatively execute additional instructions if the memory location contains a second value (Rajwar page 295 col 1), and causes the processor to start executing instructions from an address indicated by the second operand if a mis-speculation occurs (Lam page 187 TRY instruction);

Note the {addr} value.

And a speculation termination instruction that takes first and second operands and causes the processor to begin retiring the additional instructions if the additional instructions have been speculatively executed (Lam page 187 COMMIT instruction).

16. Regarding claim 7, Rajwar/Lam discloses the processor of claim 6, wherein the mis-speculation comprises an interrupt (Lam page 187 section 3.2 first column.).

Note "error-detected", which will interrupt the speculative execution.

17. Regarding claim 14, Rajwar/Lam discloses the method of claim 11, wherein said effecting synchronization comprises placing in an out-of-order execution management unit of a processor (see below),

Note that the use of speculative lock acquisition is used to facilitate out-of-order execution

At least one machine instruction that limits when other machine instructions are retired from the out-of-order execution management unit (Lam page 187 COMMIT and ABORT instructions).

18. Regarding claim 19, Rajwar/Lam discloses the article of claim 16, wherein said effecting synchronization comprises placing in an out-of-order execution management unit of a processor (see below),

Note that the use of speculative lock acquisition is used to facilitate out-of-order execution

At least one machine instruction that limits when other machine instructions are retired from the out-of-order execution management unit (Lam page 187 COMMIT and ABORT instructions).

19. Regarding claim 21, Rajwar/Lam discloses a machine-implemented method comprising: speculatively executing machine instructions (Rajwar page 295 col 1), including a memory access instruction (Rajwar page 296 col 1),

Note the use of load and test instructions.

In a processing system to effect synchronization between parallel processes (Rajwar page 295 col 1); retiring the speculatively executed machine instructions (Lam page 187 section 3.2 col 2 COMMIT instruction); and maintaining cache coherence in the processing system during said executing and said retiring to identify a mis-

speculation to effect the synchronization between the parallel processes (Rajwar page 295 col 2 first line).

20. Regarding claim 22, Rajwar/Lam discloses the method of claim 21, wherein said maintaining cache coherence comprises providing invalidation based cache coherence (see below).

Note that the "cache coherence protocols already implemented on modern processors" (Rajwar page 295, beginning of col 2) implies the use of invalidation.

21. Regarding claim 23, Rajwar/Lam discloses the method of claim 21, wherein said speculatively executing machine instructions comprises speculatively executing machine instructions in the processing system comprising multiple processors, and the mis-speculation comprises a memory dependency violation (Rajwar page 295 col 1).

22. Regarding claim 24, Rajwar/Lam discloses the method of claim 21, wherein the mis-speculation comprises at least one of an interrupt (Lam page 187 section 3.2 first column.),

Note "error-detected", which will interrupt the speculative execution.

An external event (Lam page 187 section 3.2 first column.),

Note that the "error-detected" is considered to be external to the speculation logic.

And a memory dependency violation (Rajwar page 295 col 1).

23. Regarding claim 25, Rajwar/Lam discloses a system comprising: a processor (Rajwar page 294 section 1 col 1) having a processor architecture that provides speculative execution of machine instructions (Rajwar page 295 col 1) and exposes said speculative execution to program control through at least one machine instruction (Lam page 187 TRY instruction); and a memory coupled with the processor, the memory embodying information indicative of instructions (Rajwar page 294 figure 1),

Note that for these instructions to be read, a memory must be used.

Including the at least one machine instruction, that result in synchronization between parallel processes when performed by the processor with detection of mis-speculation (Lam page 197 TRY instruction).

24. Regarding claim 26, Rajwar/Lam discloses the system of claim 25, wherein the processor comprises a uniprocessor (Rajwar page 294 section 1 col 1).

Note that the two suggestions made are "multiprocessors" OR multithreaded architecture (implied to be in a single uniprocessor)

25. Regarding claim 27, Rajwar/Lam discloses the system of claim 25, wherein the processor comprises a multiprocessor (Rajwar page 294 section 1 col 1).

26. Regarding claim 31, Rajwar/Lam discloses the system of claim 25, wherein the at least one machine instruction comprises: a speculative execution instruction (Lam page 187 TRY instruction) that takes first and second operands,

Note: see claim 6.

Behaves as a no-op if a memory location indicated by the first operand contains a first value (Lam page 187 section 3.2), causes the processor to speculatively execute additional instructions if the memory location contains a second value (Rajwar page 295 col 1), and causes the processor to start executing instructions from an address indicated by the second operand if a mis-speculation occurs (Lam page 187 TRY instruction); and a speculation termination instruction that causes the processor to begin retiring the additional instructions if the additional instructions have been speculatively executed (Lam page 187 COMMIT instruction).

27. Regarding claim 32, Rajwar/Lam discloses the system of claim 25, further comprising an environmental sensor coupled with the processor (Lam page 187 end of section 3.2).

Note that the error detection if statement is considered to be an environmental sensor.

28. Regarding claim 33, Rajwar/Lam discloses a processing system comprising: processing means for speculatively executing machine instructions in response to a speculative execution instruction (Rajwar page 294 LOCK instruction and page 295 col

1), including means for detecting a mis-speculation (Rajwar page 295 col 1); means for treating multiple speculative instructions as a group for purposes of retirement such that the multiple speculative instructions are flushed from the processing means together (Lam page 187 COMMIT instruction or Rajwar page 295 col 1 "recovery") and execution proceeds from an address in response to a detected mis-speculation to effect synchronization between parallel processes (Lam page 187 TRY instruction).

29. Regarding claim 34, Rajwar/Lam discloses the processing system of claim 33, wherein said means for detecting a mis-speculation comprises means for maintaining cache coherence in the processing means (Rajwar page 295 col 1 last paragraph to col 2 first paragraph).

30. Claims 2-5, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajwar/Lam in view of Christie (U.S. Patent No. 6,009,512).

31. Regarding claim 2, Rajwar discloses the processor of claim 1.

Rajwar/Lam contains an out-of-order processor (as suggested by the speculative lock interface), but fails to disclose particular information about how the out-of-order system works.

Christie discloses a front end that comprises an in-order front end (Christie fig 5), and the back end comprises an out-of-order execution engine (Christie fig 5), which re-

orders the instructions (Christie col 6 line 49), and one or more execution units that perform the re-ordered instructions (Christie fig 5 references 1212A-C).

For subsequent claims, Christie also discloses a branch prediction unit.

Examiner asserts that out-of-order execution must start and end in program order, while allowing the execution units execute out-of-order execution. Consequently, an in-order front end with an out-of-order back end, as claimed, is likely an inherent aspect of the invention for Rajwar/Lam; however, in case Examiner is neglecting to consider an exception, this will be an obvious rejection. Rajwar/Lam would be motivated to utilize an in-order front end with an out-of-order back end, because this is, as one of ordinary skill in the art would have realized, a simple and efficient mechanism for out-of-order processing.

Additionally, Rajwar/Lam would be motivated to utilize a branch prediction unit. As one of ordinary skill in the art would have realized, a branch prediction unit can cause large performance increases in a processor. An invention such as Rajwar/Lam with that particular intention in mind would be particularly motivated to utilize this mechanism.

It would have been obvious at the time of the invention for one of ordinary skill in the art for the processing system of Rajwar/Lam to utilize mechanisms of Christie that were not described in great detail (so not to obscure the invention of Rajwar/Lam) such as a branch prediction unit and Christie's out-of-order processing setup.

32. Regarding claim 3, Rajwar/Lam/Christie discloses the processor of claim 2, wherein the out-of-order execution engine comprises an out-of-order execution management unit (Christie fig 5), including at least one buffer (Christie col 7 line 51), and an in-order retire-store unit (Christie col 7 lines 54-64).

33. Regarding claim 4, Rajwar/Lam/Christie discloses the processor of claim 3, wherein the at least one buffer comprises a reorder buffer (Christie col 7 lines 54-64).

34. Regarding claim 5, Rajwar/Lam/Christie discloses the processor of claim 1, wherein the front end comprises a fetch-decode unit (see below)

Note that it is an inherent aspect of the referenced invention to have a fetch-decode unit. In order for the instructions to be processed, they must be fetched and decoded.

And a branch prediction unit (Christie col 6 line 35).

35. Regarding claim 8, Rajwar/Lam/Christie discloses a processor comprising: a front end that obtains instructions; and a back end that provides speculative execution of the instructions (Christie fig 5) wherein the processor has an instruction set architecture including speculative execution control circuitry that handles a speculative execution instruction (Rajwar page 295 col 1) and a speculation termination instruction (Lam COMMIT instruction).

36. Regarding claim 9, Rajwar/Lam/Christie discloses the processor of claim 8, wherein the front end comprises an in-order front end, and the back end comprises an out-of-order execution engine (Christie Fig 5), which re-orders the instructions (Christie col 6 line 49), and one or more execution units that perform the re-ordered instructions (Christie fig 5 references 1212A-C).

37. Regarding claim 10, Rajwar/Lam/Christie discloses the processor of claim 8, wherein the speculative execution instruction comprises an instruction that takes first and second operands,

Note: see claim 6.

Causes the processor to speculatively execute additional instructions if a memory location contains a value (Lam page 187 section 1 col 1), and causes the processor to start executing instructions from an address indicated by the second operand if a mis-speculation occurs (Lam page 187 col 2 TRY {addr}), and the speculation termination instruction comprises an instruction that causes the processor to begin retiring the additional instructions (Lam page 187 col 2 COMMIT instruction).

38. Claims 13, 18 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajwar in view of common prior art.

39. Regarding claim 13, Rajwar discloses the method of claim 11.

Rajwar fails to disclose synchronization comprises translating at least one high-level software instruction into at least one machine instruction that controls speculative execution in a processor.

Examiner asserts that the use of a high-level language is extremely common in the art. Rajwar would be motivated to utilize this strategy to simply the code writing process for a programmer at a high level language, and allow a compiler/assembler put the language in machine code for the processor to read.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the machine instructions in the processing system of Rajwar, and have them translated from a high-level language.

40. Regarding claim 18, Rajwar discloses the article of claim 16. See claim 13 above.

41. Regarding claim 28, Rajwar discloses the system of claim 27.

Rajwar fails to disclose that the multiprocessors are in a single die.

Examiner asserts that placing multiple processing units on a single die is extremely common in the art and allows for faster, cheaper and more power effective processing systems.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow all the processors of Rajwar to be on a single die, an expected result considering that, as disclosed by Rajwar, all processors have a shared memory.

42. Claims 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajwar/Lam in view of common prior art.

43. Regarding claims 29 and 30, Rajwar/Lam discloses the system of claim 25, further comprising: a communication interface (Rajwar page 294 section 1 col 1);

Note that the processing system is considered to be a communication interface.

Rajwar fails to disclose a virtual machine, including a java virtual machine.

Examiner asserts that the use of a java virtual machine in a processing system is extremely common in the art and gives the processing system added security by preventing information inside the machine to be accessed outside the machine. Portability of code is another potential motivation.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the system of Rajwar/Lam utilize a java virtual machine.

Conclusion

44. The following is text cited from 37 CFR 1.11(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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